# C. U. SHAH UNIVERSITY
## Wadhwan City

**FACULTY OF**: - Technology and Engineering
**DEPARTMENT OF**: - Electronics & Communication Engineering
**SEMESTER**: VII
**CODE**: - **4TE07VLT1**
**NAME**: – **VLSI Technology (VLT)**

**Teaching & Evaluation Scheme**:-

| Subject Code | Subject Name | Teaching Schemes (Hours) | | | | Credits | Evaluation Schemes | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Theory | | | | Practical (Marks) | | | Total |
| | | | | | | | | | | | Internal | | University | |
| | | Th | Tu | Pr | To | | Sessional Exam | | University Exam | | Pr | TW | Pr | |
| | | | | | | | Marks | Hours | Marks | Hours | | | | |
| 4TE07VLT1 | VLSI Technology (VLT) | 04 | 00 | 02 | 06 | 05 | 30 | 1.5 | 70 | 3.0 | --- | 20 | 30 | 150 |

**Objectives:-**

- In this course, student will study static &dynamic logic, combinational and sequential circuits, propagation delay, transistor sizing, MOS IC fabrication, layout and design rules, stick diagrams.

**Prerequisite:-**

- Students should have a firm grasp Digital Electronics in third semesters. The basic concepts of mathematics must be clear.

**Course Outline:-**

| Sr. No. | Course Content | Hours |
|---|---|---|
| 1 | **Introduction:** Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, Package technology, Computer aided design technology. | 4 |
| 2 | **Fabrication of MOSFET:** Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design. | 4 |
| 3 | **MOS Transistor:** Introduction, The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure & Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling, MOSFET capacitances | 8 |
| 4 | **MOS inverters: Static characteristics:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement & Depletion type MOSFET load), CMOS Inverter | 8 |

| | | |
|---|---|---|
| **5** | **MOS inverters Switching characteristics and Interconnect Effects:**<br>Introduction, delay-time definitions, calculation of delay times, inverter design with delay constraints, estimation of interconnect parasitic, calculation of interconnect delay, switching power dissipation of CMOS Inverters. | **8** |
| **6** | **Combinational MOS Logic circuits :**<br>Introduction, MOS logic circuits with Depletion NMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs) | **6** |
| **7** | **Sequential MOS Logic circuits :**<br>Introduction, Behaviour of Bistable elements, The SR latch circuit, Clocked latch & Flip-flop circuit, CMOS D-latch & Edge-triggered flip-flop | **5** |
| **8** | **Dynamic Logic Circuits :**<br>Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-performance Dynamic CMOS circuits | **8** |
| **9** | **Chip Input and Output Circuits :**<br>On chip Clock Generation and Distribution, Latch –Up and its Prevention | **4** |
| **10** | **Design for testability :**<br>Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques, built-in Self Test (BIST) techniques, current monitoring $I_{DDQ}$ test | **5** |

**Learning Outcomes:-**

After the successful completion of the course, students will be able to

- Use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnection.
- Create models of moderately sized CMOS circuits that realize specified digital functions.
- Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
- Understanding of the characteristics of CMOS circuit construction and the comparison between different state-of-the-art CMOS technologies.

**Books Recommended:-**


1. CMOS Digital Integrated circuits – Analysis and Design ,**Sung – Mo Kang, Yusuf Leblebici**,
   Tata McGraw-Hill, Third Edition.
2. Basic VLSI Design, **Pucknell and Eshraghian**, Pearson Education Inc.3rd edition.
3. Introduction to VLSI Systems , **Mead C & Conway**, Addison Wesley
4. Digital Integrated Circuits: A Design Perspective, **Jan M. Rabaey**, Pearson Education Inc.